What is claimed is:

1. A mask ROM comprising:

a substrate where a memory cell array region and a segment select region are defined;

first and second trenches respectively formed at the outer portion of the memory cell array region and at the outer portion of a buried layer formation region of the segment select region;

an element isolating film and an isolating pattern respectively filling up the first and second trenches;

a plurality of buried layers aligned on the substrate in a first direction by a predetermined interval, and surrounded by the isolating pattern; and

a plurality of gates aligned in a second direction to cross the buried layers in an orthogonal direction.

2. The mask ROM according to claim 1, wherein the first and second trenches have a depth of 3000 to 4000Å from the surface of the substrate.

3. The mask ROM according to claim 1, further comprising:

a protective film for covering the whole substrate including the gates;

a contact formed in the protective film, for partially exposing the buried layer of the segment select region; and

a bit line for covering the contact.

4. A method for fabricating a mask ROM comprising the steps of:

providing a substrate where a memory cell array region and a segment select region are defined;

forming an element isolating film and an isolating pattern at the outer portion of the memory cell array region and at the outer portion of a buried layer formation region of the segment select region;

forming a plurality of buried layers aligned over the resultant structure in a first direction by a predetermined interval, and surrounded by the isolating pattern; and

forming a plurality of gates aligned in a second direction to cross the buried layers in an orthogonal direction.

5. The method according to claim 4, wherein the step for forming the element isolating film and the isolating pattern comprises the steps of:

forming first and second trenches at the outer portion of the memory cell array region and at the outer portion of the buried layer formation region of the segment select

region;

forming an insulating layer on the substrate having the first and second trenches; and

etching the insulating layer.

6. The method according to claim 5, wherein the insulating layer is etched according to an etch back process or a chemical mechanical polishing process.

7. The method according to claim 4, wherein the step for forming the buried layers comprises the steps of:

forming a pad oxide film and a nitride film on the substrate having the element isolating film and the isolating pattern;

forming a mask pattern on the nitride film to cover the buried layer formation region;

exposing the substrate by removing the nitride film and the pad oxide film by using the mask pattern;

implanting impurities to the exposed substrate by using the mask pattern and the isolating pattern as a blocking mask; and

removing the mask pattern.

8. The method according to claim 4, wherein the first and second trenches have a depth of 3000 to 4000Å from the

surface of the substrate.

9. The method according to claim 4, further comprising the steps of:

forming a protective film on the substrate having the gates;

forming a contact to partially expose the buried layer of the segment select region, by etching the protective film; and

forming a bit line to cover the contact.